FIG. 1

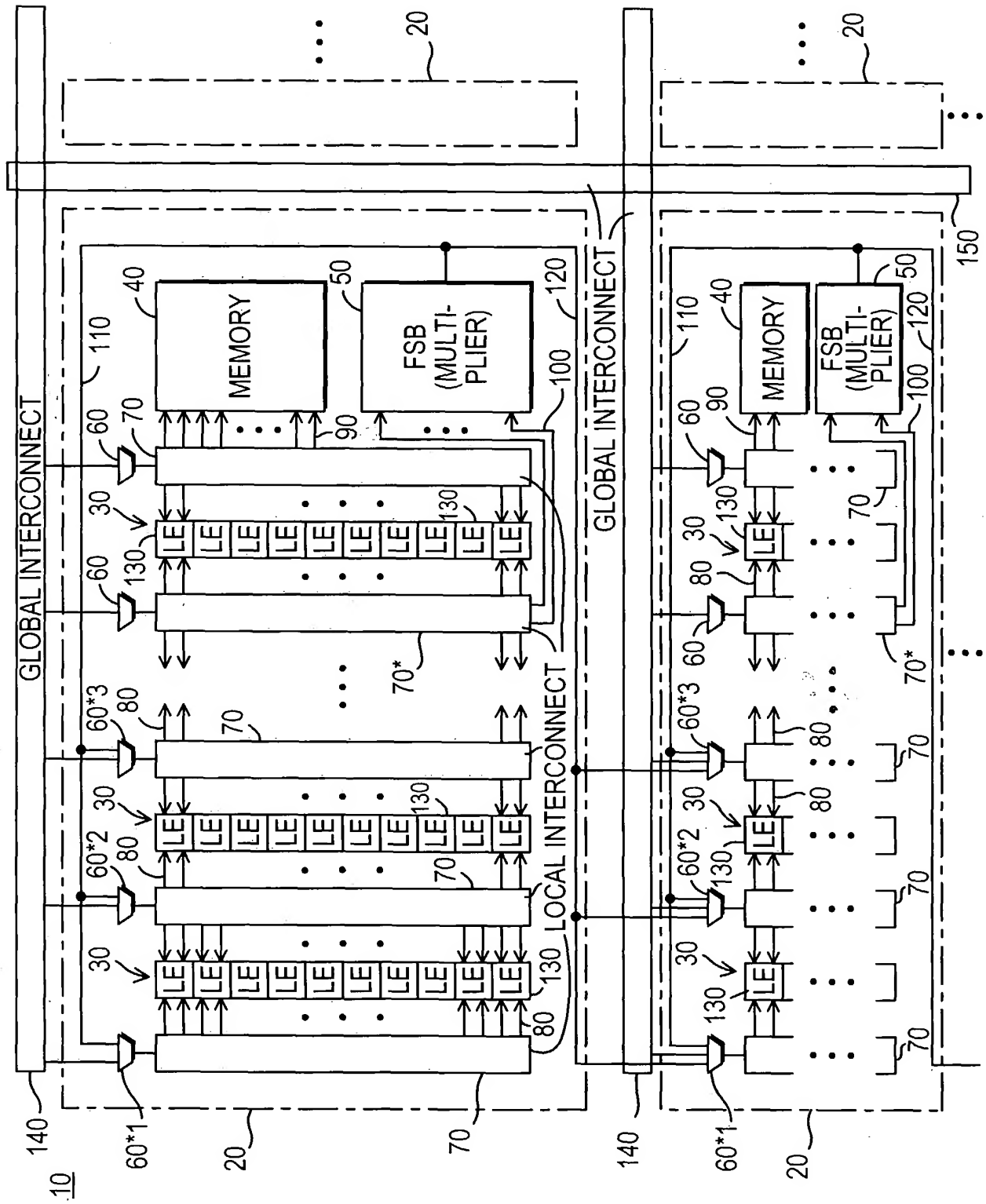
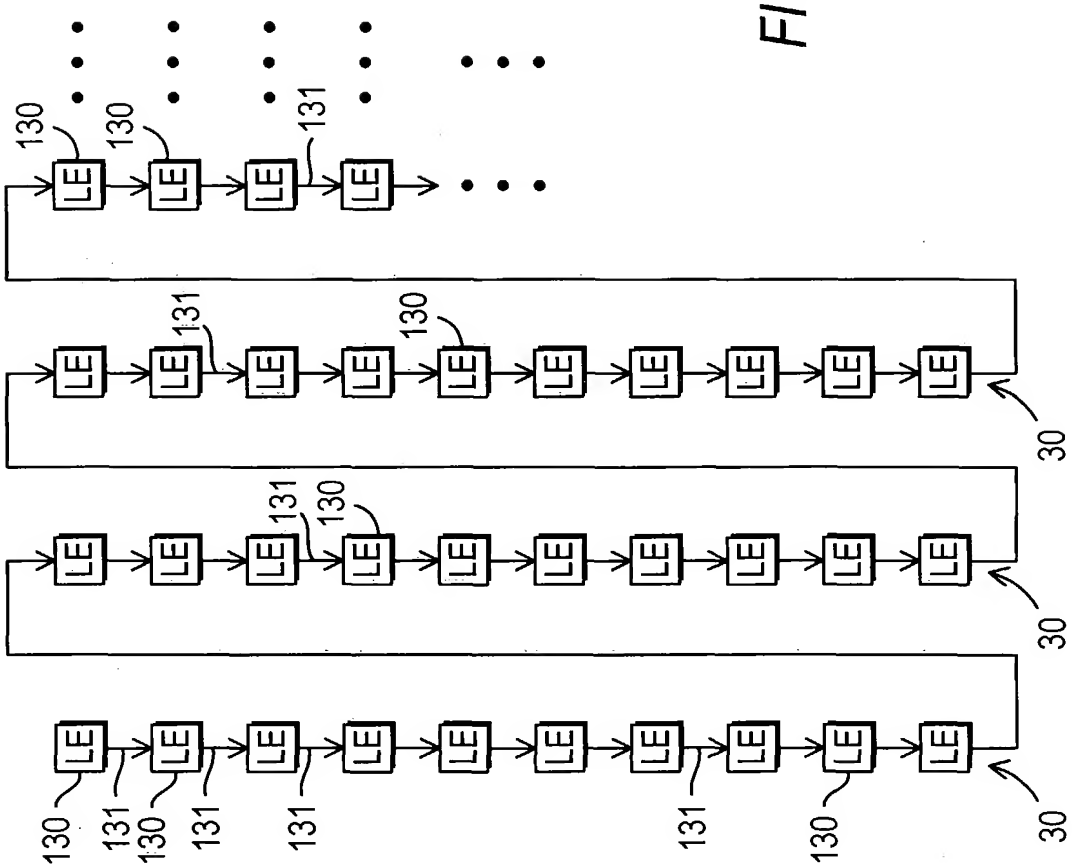

GLOBAL INTERCONNECT
GLOBAL INTERCONNECT
LOCAL INTERCONNECT
MEMORY
FSB (MULTI-PLIER)
MEMORY
FSB (MULTI-PLIER)
LE
10
20
30
40
50
60
60*1
60*2
60*3
70
70*
80
90
100
110
120
130
140
150

FIG. 1A



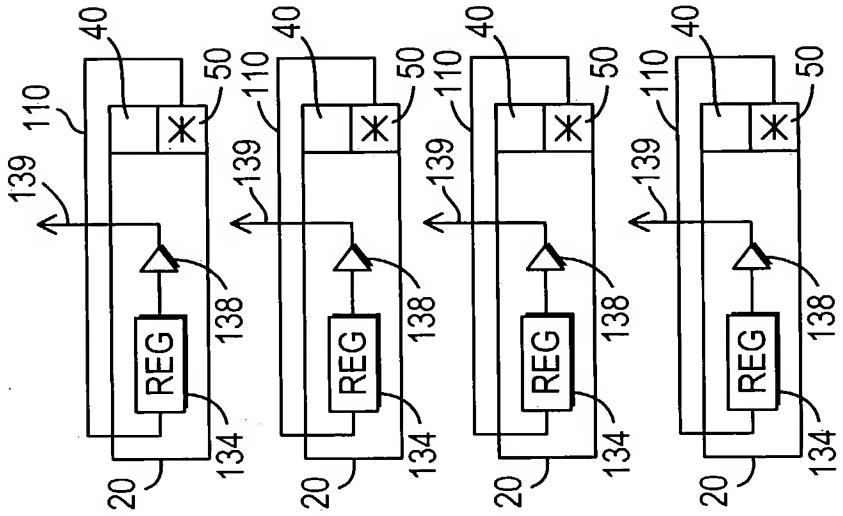


FIG. 3

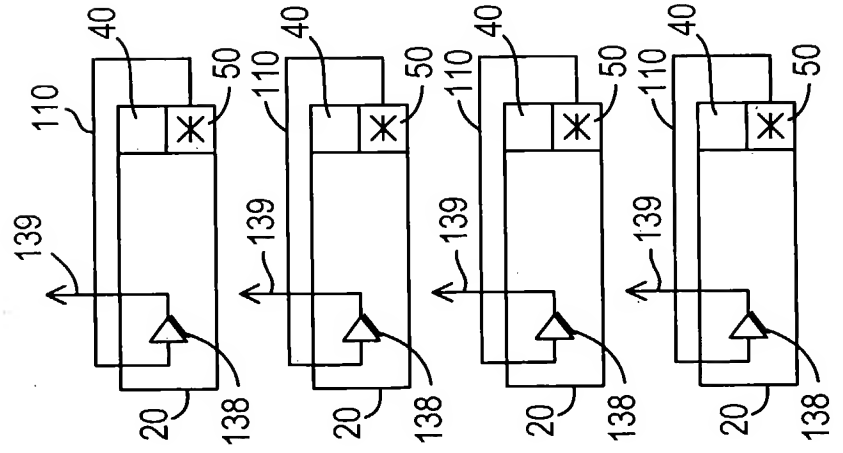


FIG. 2

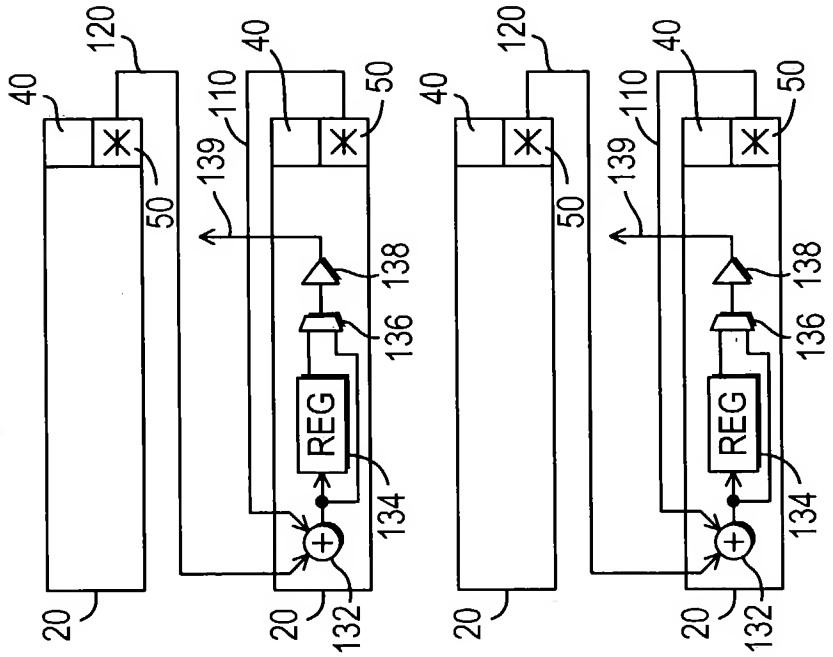

40
120
50
20
110
139
138
136
REG
134
132

FIG. 5

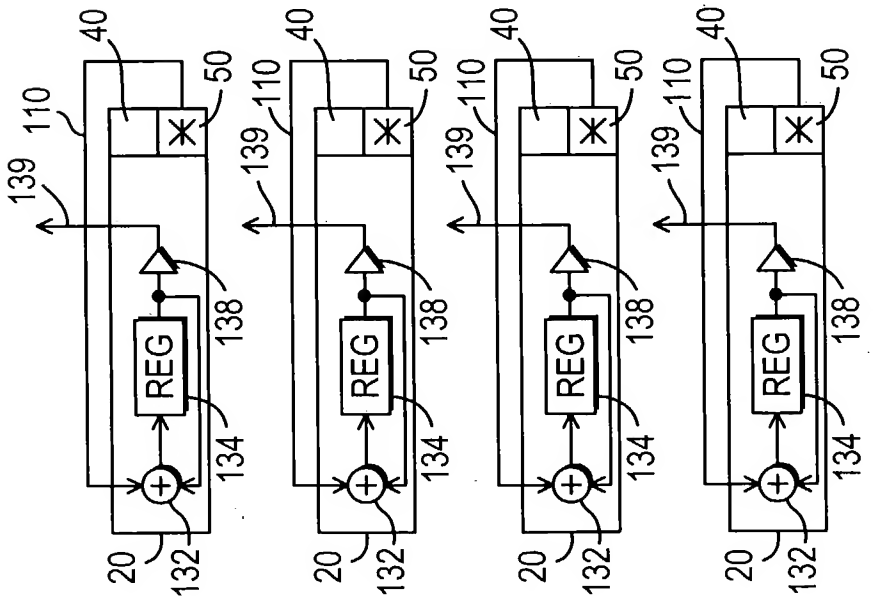

40
110
139
50
138
REG
134
20
132

FIG. 4

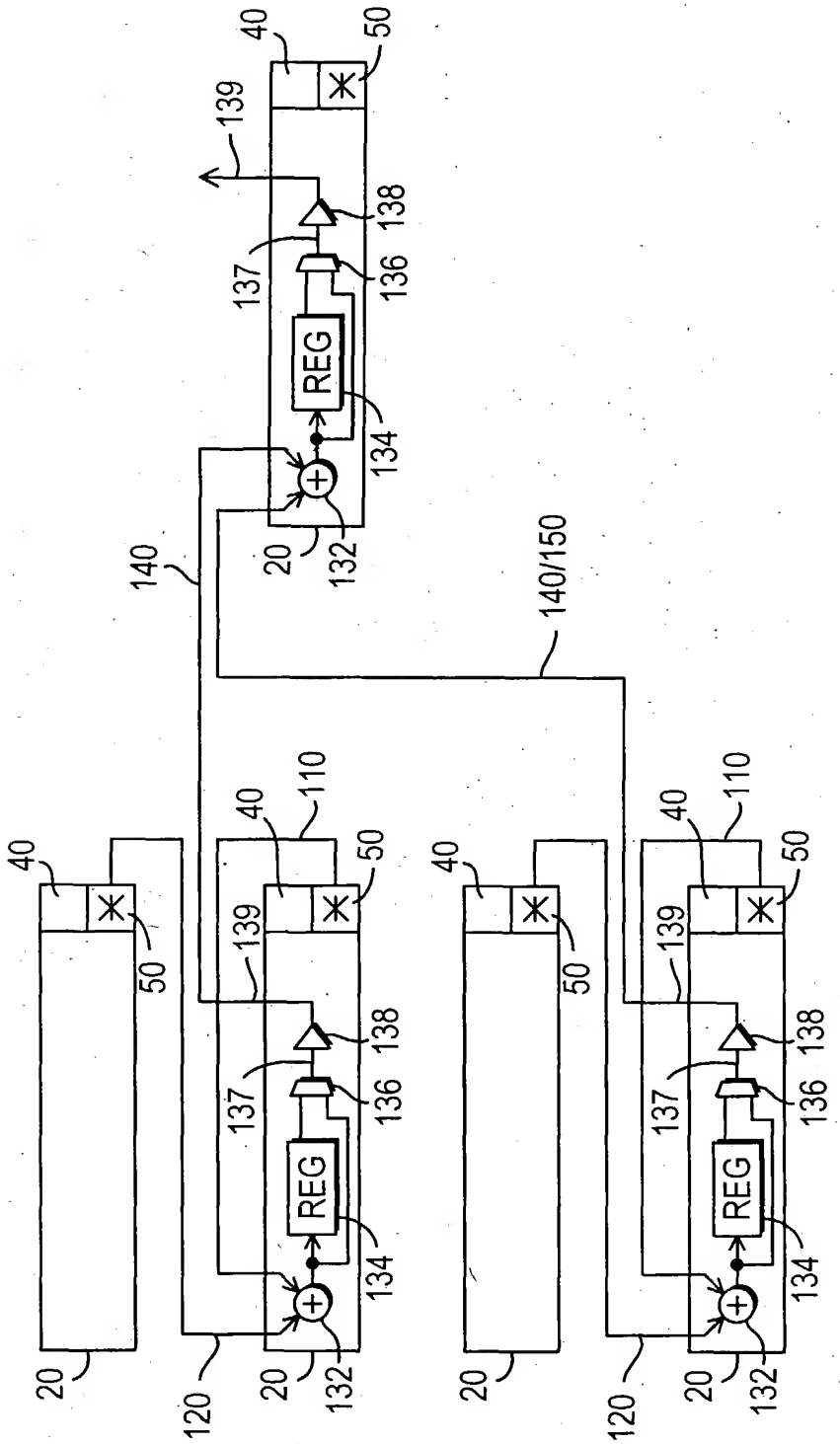


FIG. 6

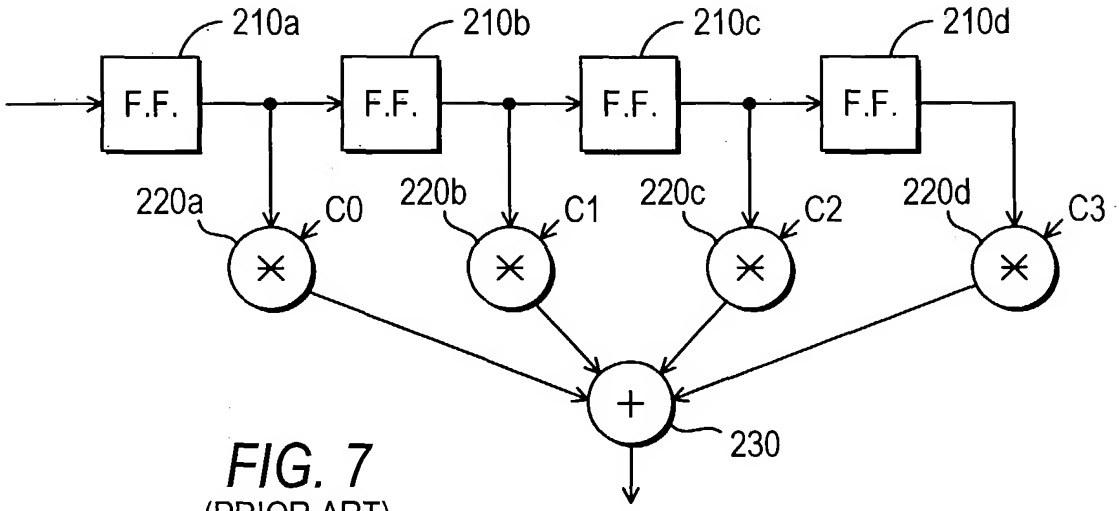


FIG. 7
(PRIOR ART)

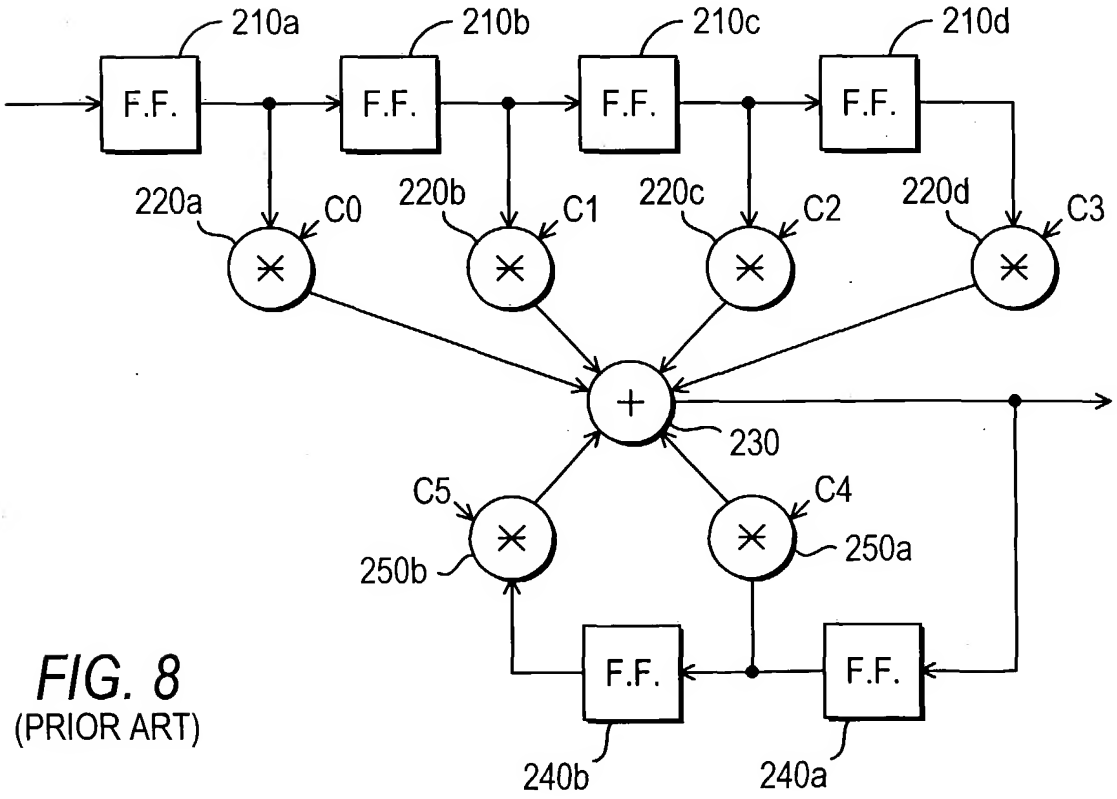


FIG. 8
(PRIOR ART)

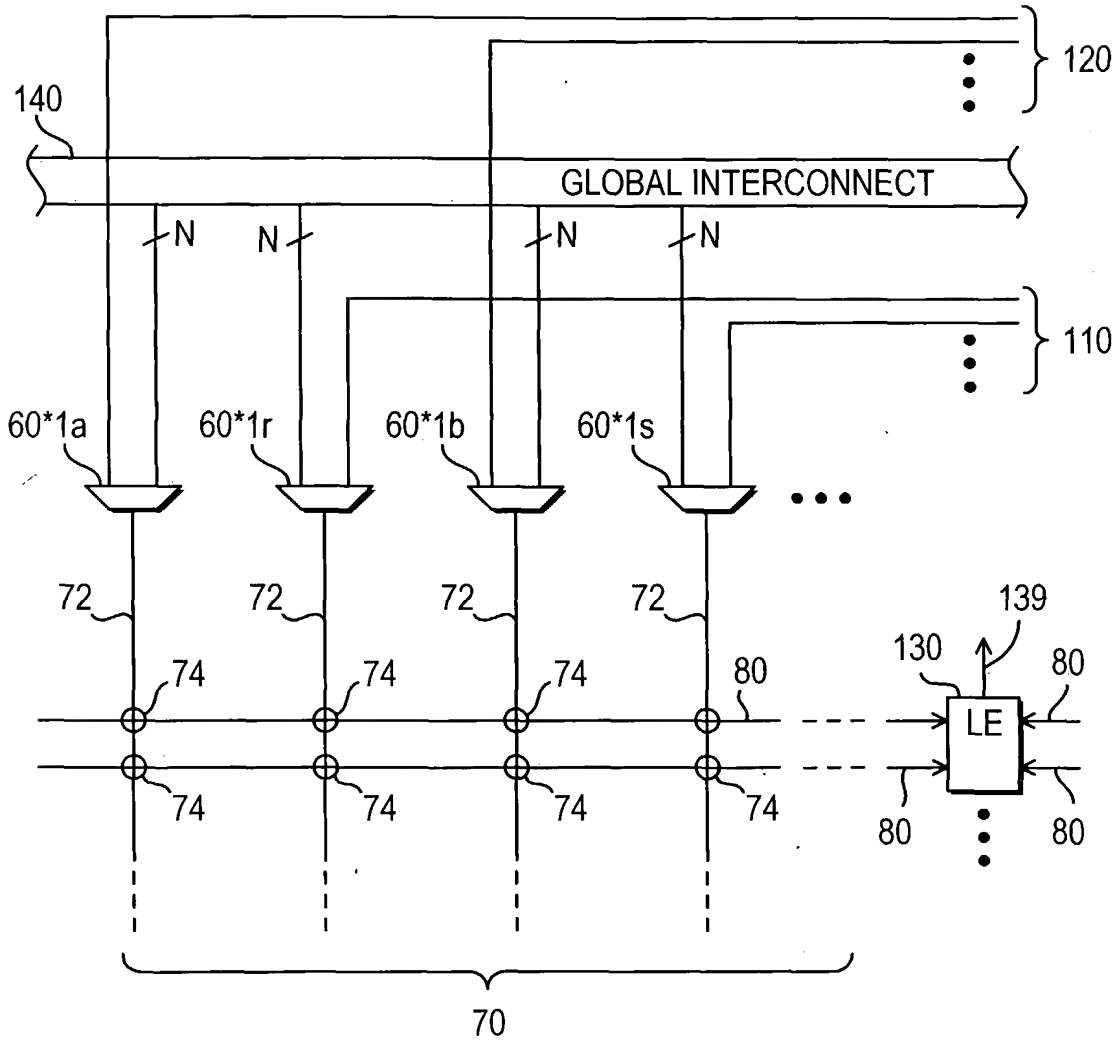

120
140
GLOBAL INTERCONNECT
N
N
N
N
110
60*1a
60*1r
60*1b
60*1s
72
72
72
72
139
130
80
74
74
74
80
LE
74
74
74
74
80
80
70

FIG. 9

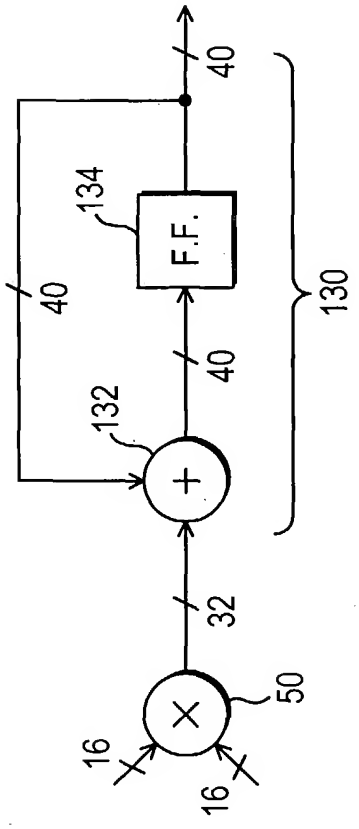


FIG. 10

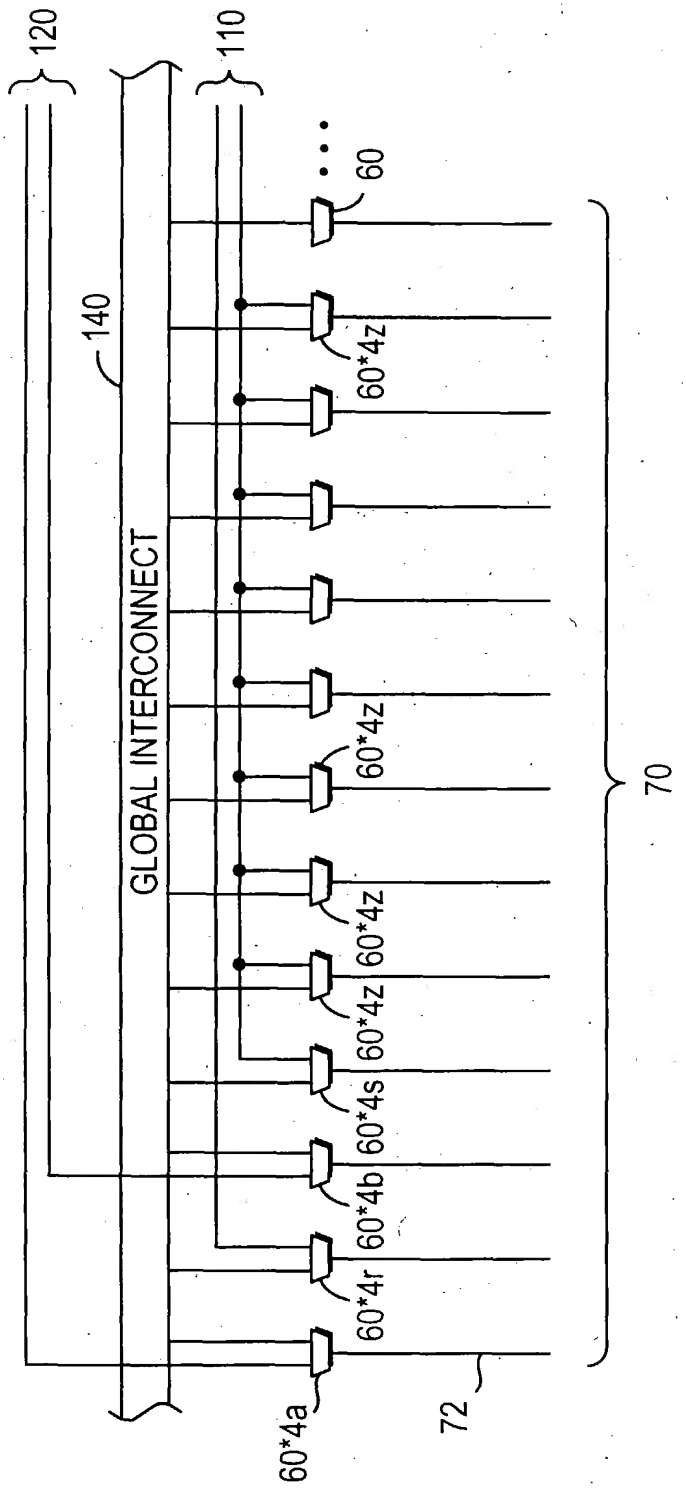

120
110
140
GLOBAL INTERCONNECT
60
60*4z
60*4z
60*4z
60*4z
60*4s
60*4b
60*4r
60*4a
70
72

FIG. 11

TWO'S COMPLEMENT	
DECIMAL VALUE	TWO'S COMPLEMENT REPRESENTATION
⋮	⋮
+3	• • • 0 0 0 0 1 1
+2	• • • 0 0 0 0 1 0
+1	• • • 0 0 0 0 0 1
0	• • • 0 0 0 0 0 0
-1	• • • 1 1 1 1 1 1
-2	• • • 1 1 1 1 1 0
-3	• • • 1 1 1 1 0 1
-4	• • • 1 1 1 1 0 0
⋮	⋮

FIG. 12
(PRIOR ART)

ONE'S COMPLEMENT	
DECIMAL VALUE	ONE'S COMPLEMENT REPRESENTATION
⋮	⋮
+3	• • • 0 0 0 0 1 1
+2	• • • 0 0 0 0 1 0
+1	• • • 0 0 0 0 0 1
0	• • • 0 0 0 0 0 0
-1	• • • 1 1 1 1 1 0
-2	• • • 1 1 1 1 0 1
-3	• • • 1 1 1 1 0 0
-4	• • • 1 1 1 0 1 1
⋮	⋮

FIG. 13
(PRIOR ART)

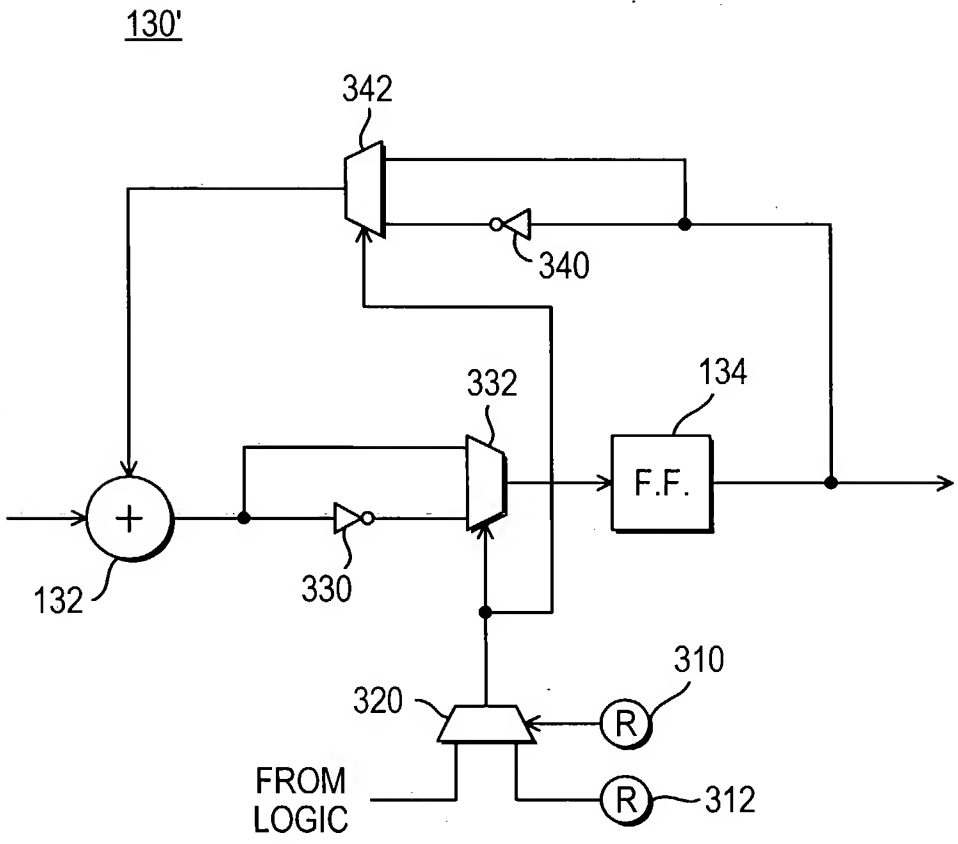


FIG. 14

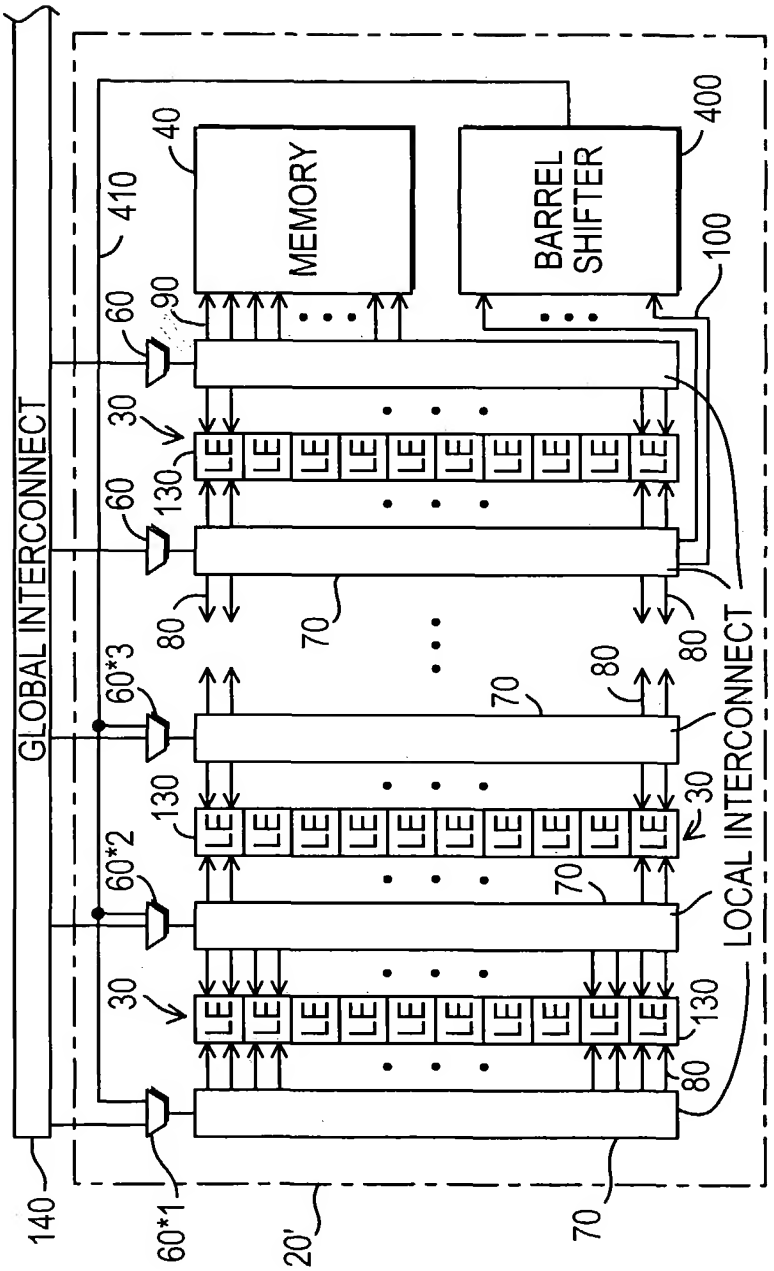

GLOBAL INTERCONNECT
MEMORY
BARREL SHIFTER
LOCAL INTERCONNECT
LE
40
400
410
100
60
90
30
130
80
70
60*3
60*2
60*1
140
20'

FIG. 15

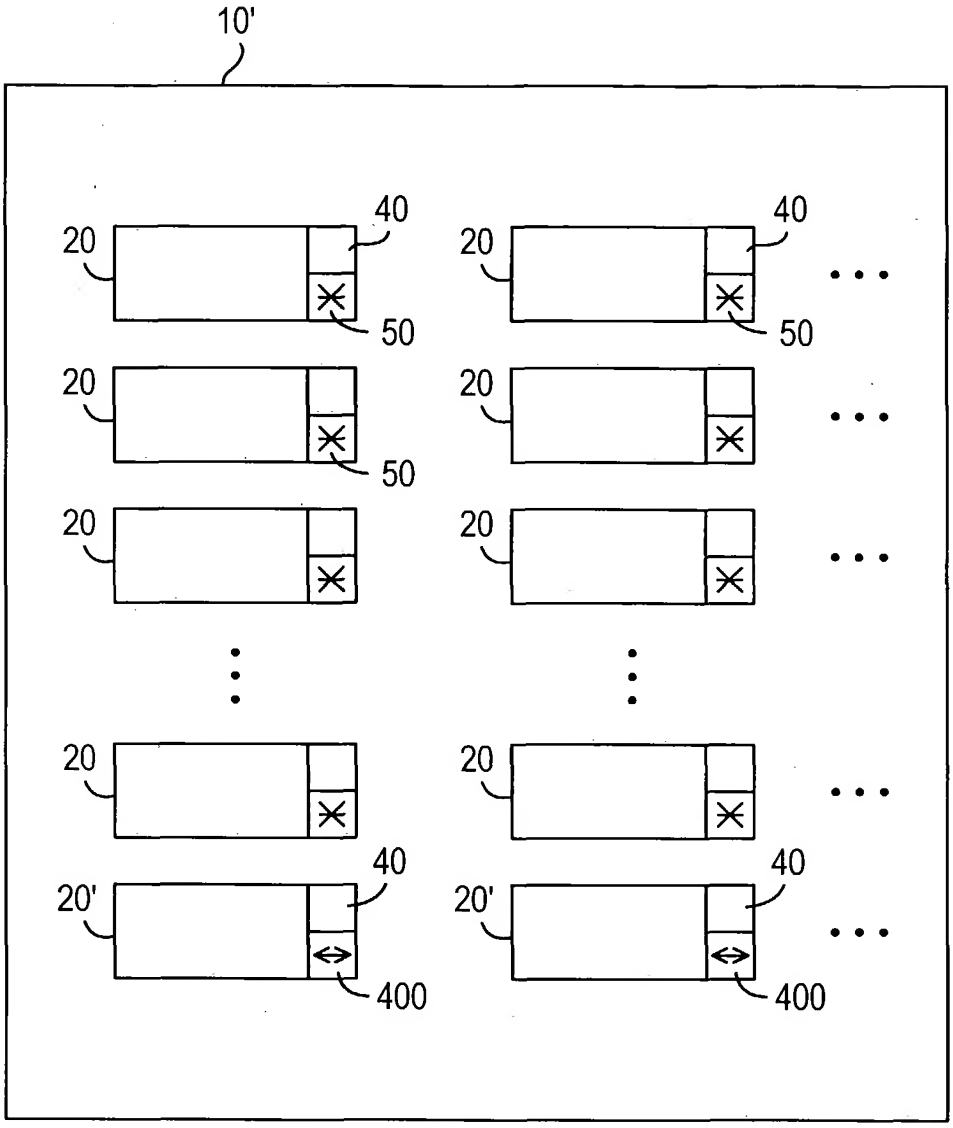


FIG. 16

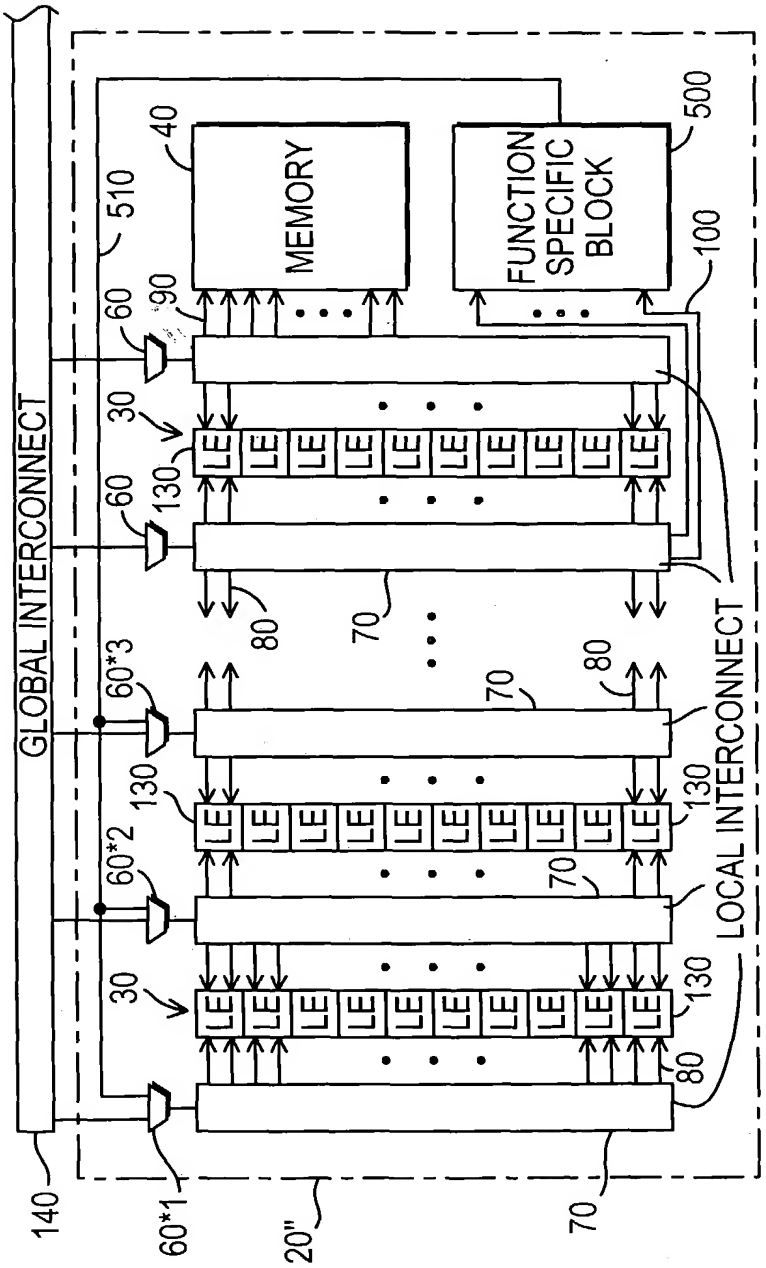

GLOBAL INTERCONNECT
MEMORY
FUNCTION SPECIFIC BLOCK
LOCAL INTERCONNECT
LE
40
500
510
100
90
60
30
130
80
70
60*3
60*2
60*1
140
20"

FIG. 17

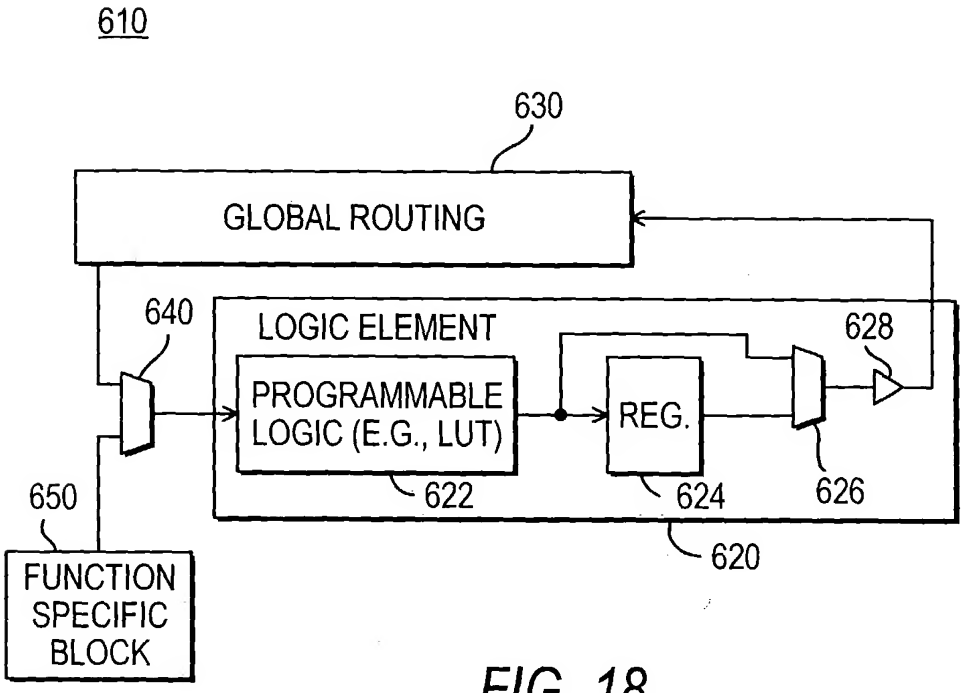

610
630
GLOBAL ROUTING
640
LOGIC ELEMENT
628
PROGRAMMABLE LOGIC (E.G., LUT)
REG.
650
622
624
626
620
FUNCTION SPECIFIC BLOCK

FIG. 18

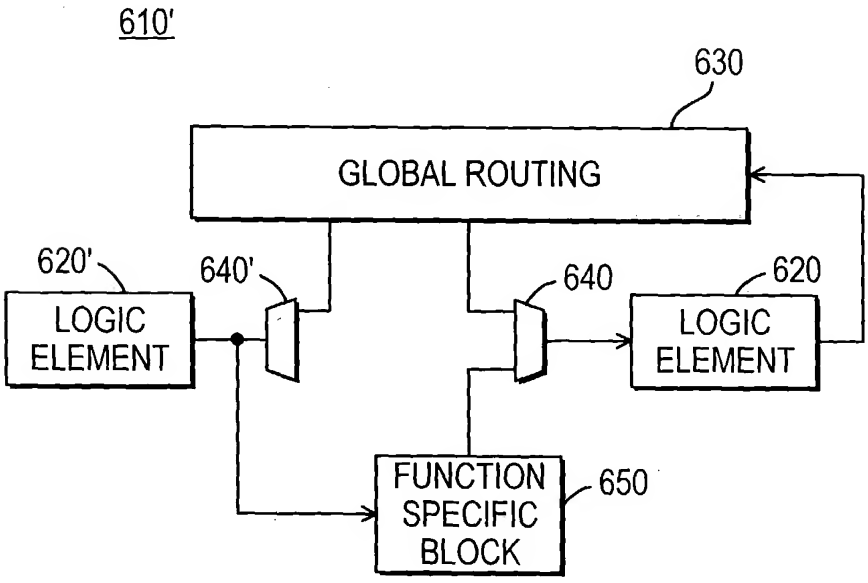

610'
630
GLOBAL ROUTING
620'
640'
640
620
LOGIC ELEMENT
LOGIC ELEMENT
FUNCTION SPECIFIC BLOCK
650

FIG. 19

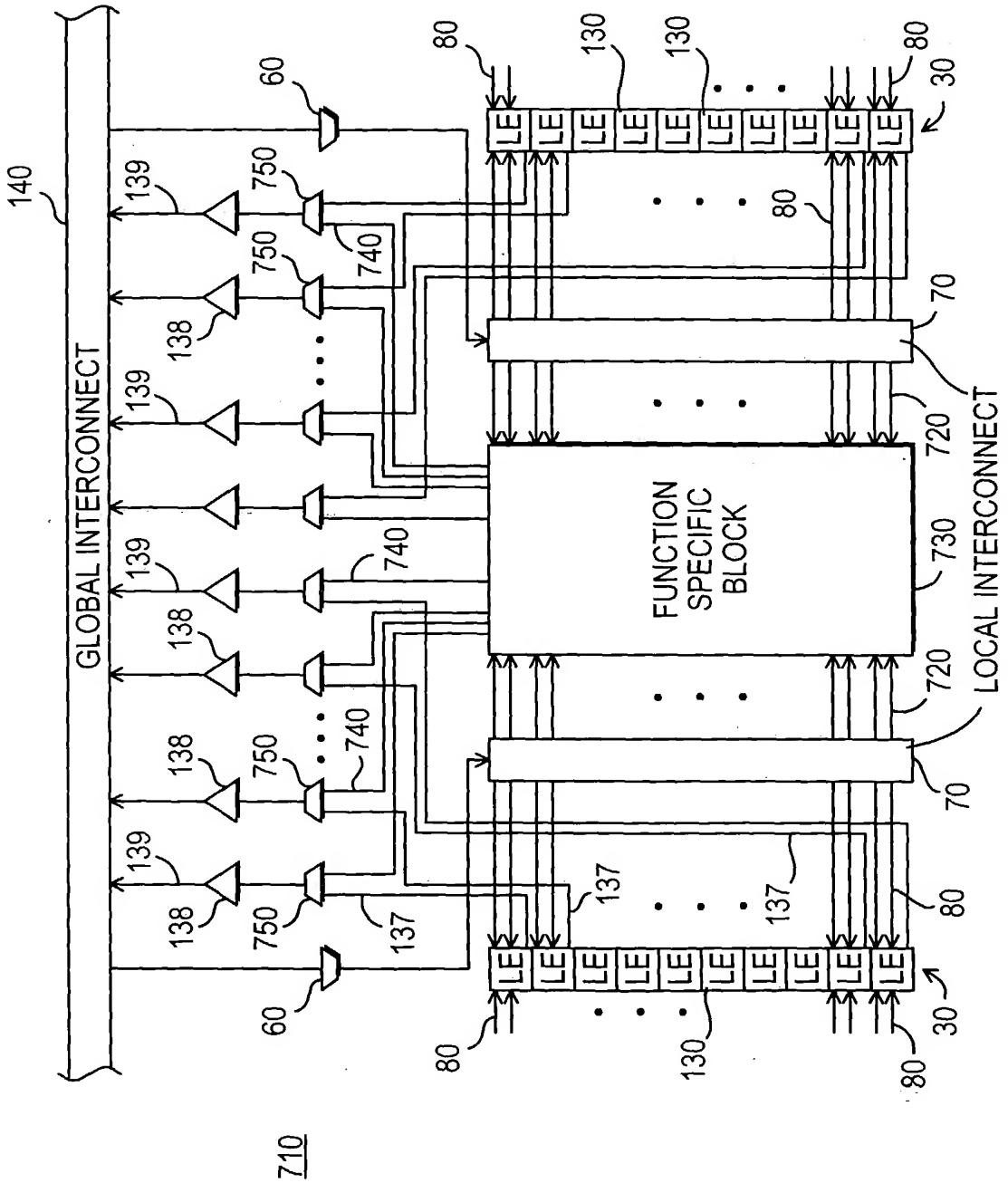
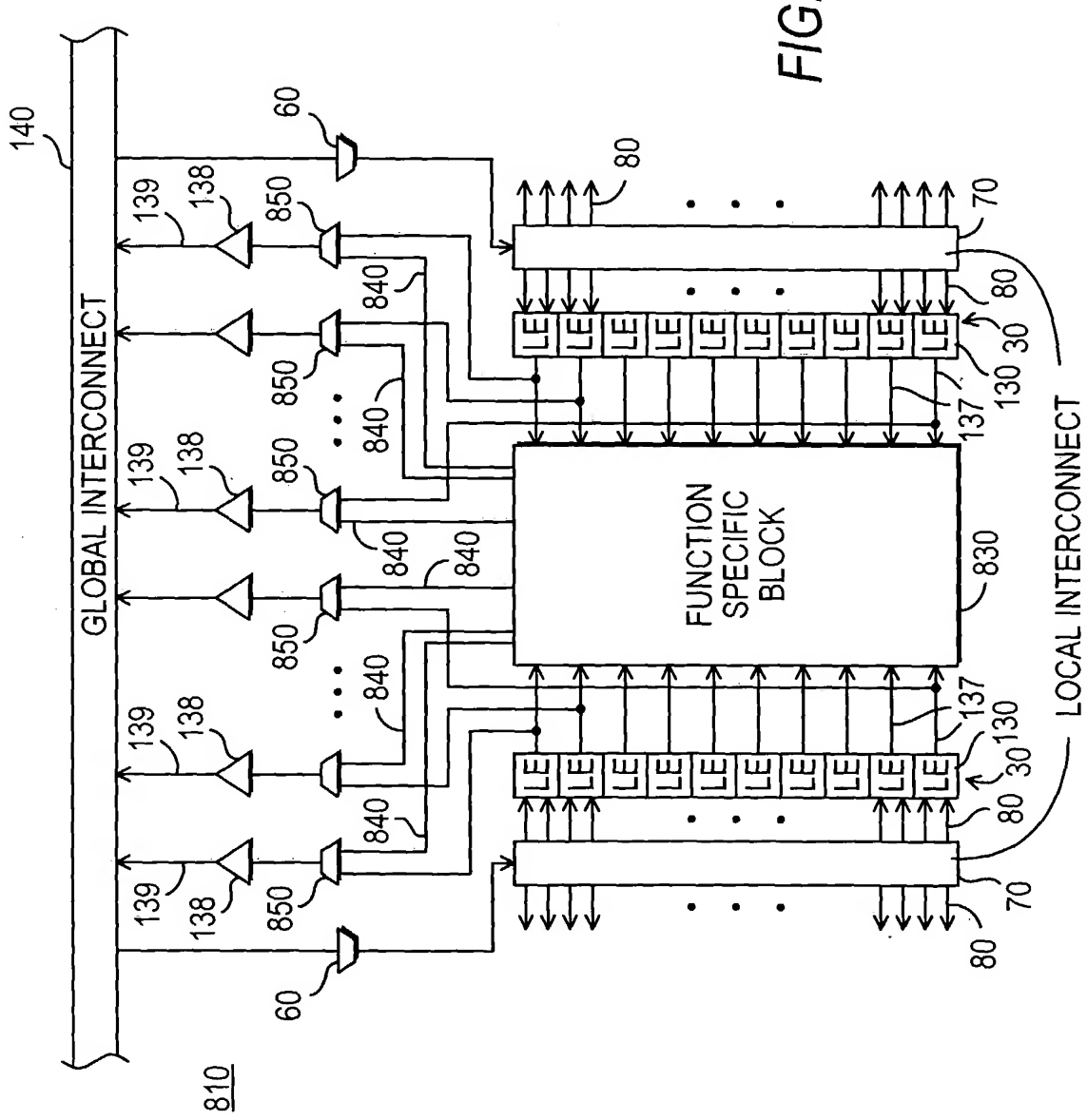

GLOBAL INTERCONNECT
LOCAL INTERCONNECT
FUNCTION SPECIFIC BLOCK
LE
140
139
138
137
750
740
730
720
70
80
130
60
30
710

FIG. 20

FIG. 21


GLOBAL INTERCONNECT
LOCAL INTERCONNECT
FUNCTION SPECIFIC BLOCK
LE
140
60
80
70
30
130
137
139
138
850
840
830
810

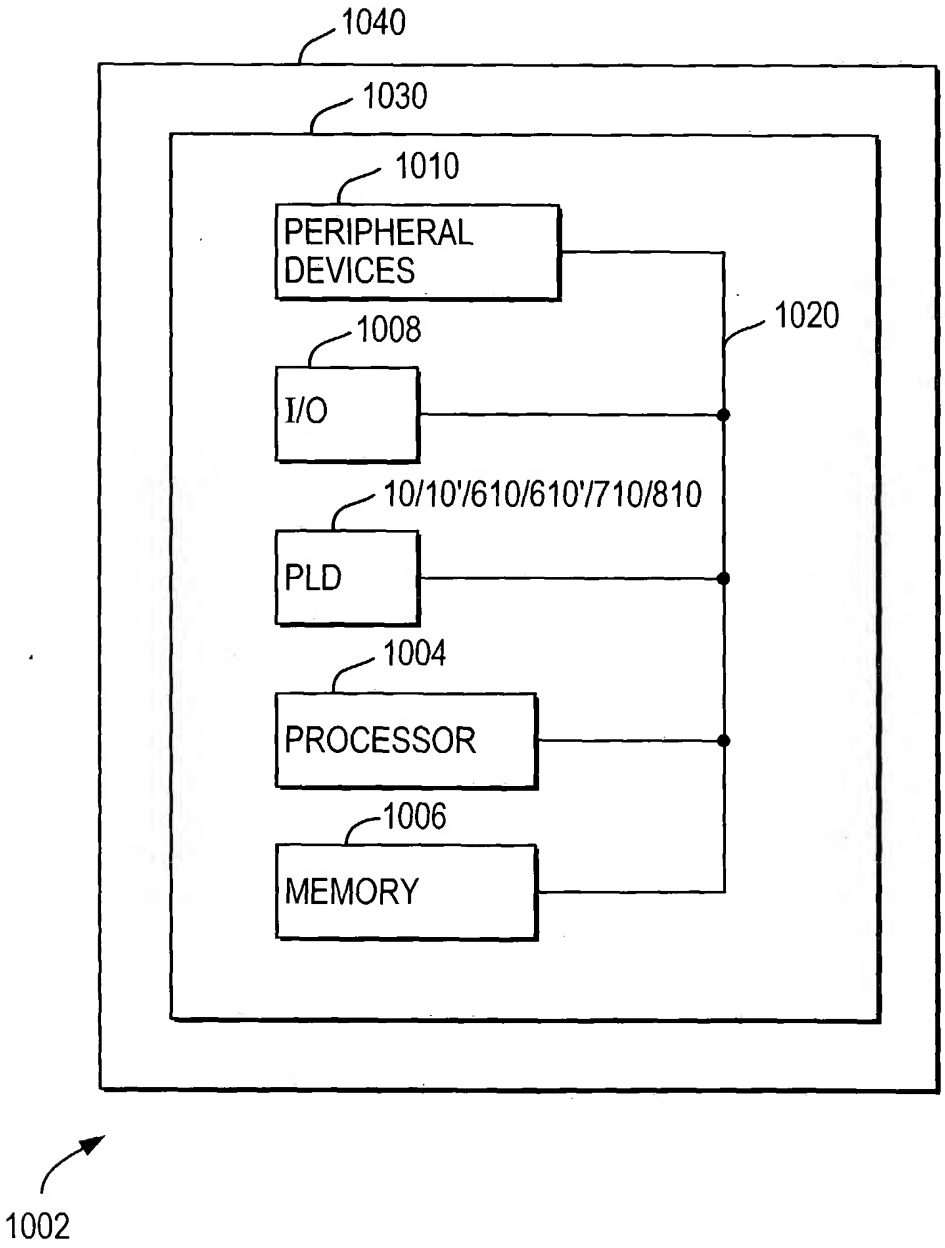

1040
1030
1010
PERIPHERAL DEVICES
1020
1008
I/O
10/10'/610/610'/710/810
PLD
1004
PROCESSOR
1006
MEMORY
1002

FIG. 22